REMARKS

These remarks are in response to the First Office Action dated March 20, 2007 (Office Action). As this reply is timely filed, no fee is believed due. Claims 1, 9, 12, 14, 20, and 22 have been amended. Claim 21 has been cancelled. Claims 1-20 and 22 now are pending. Support for these amendments can be found in paragraphs 17, 21-23, and throughout the Applicants' specification. No new matter has been introduced.

Within these remarks, the Applicants may discuss more than one claim concurrently or more than one element (limitation) from different claims concurrently. This "grouping" of claims and/or elements of claims is solely to track the grouping of claims and reasoning set forth in the Office Action. Though one or more elements of different claims may refer to similar or the same subject matter, the concurrent treatment of two or more claims and/or features of different claims does not, in and of itself, imply that such claims and/or features do refer to the same subject matter.

Rejections under 35 U.S.C. § 101

Claims 20-22 have been rejected under 35 U.S.C. § 101 for being directed to non-statutory subject matter. Claims 20 and 22 have been amended to recite a computer program product that comprises a computer-usable medium comprising a bitstream that configures a programmable logic device (PLD). Claim 21 has been cancelled. Accordingly, withdrawal of the 35 U.S.C. § 101 rejection of claims 20 and 22 is respectfully requested.

Rejections under 35 U.S.C. § 102(b)

Claims 1, 4-12, 14, and 20-22 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,356,637 to Garnett (Garnett). Garnett, however, does not teach or suggest each limitation recited in these claims.

As amended, claim 1 recites "a microcontroller within the PLD for receiving an encrypted bitstream." The Office Action contends that Garnett teaches a microcontroller in FIG. 1, at items 3 and 9. Item 3 refers to the "functional portion" of the PLD. In describing item 3 of FIG. 1, Garnett does not disclose that the "functional

portion" of the PLD (item 3) is, or includes, a microcontroller. Item 9 is a communication link that is external to the PLD. Thus, neither item 3 nor item 9 teaches or suggests a microcontroller as recited by claim 1.

Claim 1 further recites "a configuration data register in the PLD, wherein the configuration data register cannot be read by the microcontroller after the decryptor is used." The Office Action contends that Garnett teaches the configuration data register in FIG. 1; in FIG. 6 at item 3 and item 17; at column 5, lines 52-60; and at column 7, lines 5-13. First, as noted, Garnett does not teach that the functional portion of the PLD includes microcontroller.

Second, the cited portions of Garnett do not teach that the configuration data register cannot be read by the microcontroller after the decryptor is used. For example, column 5, lines 52-60, referring to item 3 of FIG. 1, teach that the functional portion of the PLD is formed of volatile elements based on SRAM technology. Column 7, lines 5-13, referring to items 3 and 17 of FIG. 6, state "[b]y contrast to the preceding embodiments, dedicated decryption circuitry is not provided, but rather the decryption function is subsumed in the functional portion 3 of the FPGA and in a state machine 17." This passage teaches that the function portion of the PLD can include the decryption function, but does not teach or suggest a configuration register as recited in claim 1.

Garnett does disclose a "disabling element" that can "bar external communication to the decryption key storage 56 from the decryption key input 13 after the disabling element 14 has been actuated." The decryption key storage, however, is not the configuration data register of the PLD. Garnett does not teach or suggest a mechanism that would prevent one from acquiring decrypted configuration data stored in the configuration data register of the PLD.

Claims 9 and 12 include similar features that are not taught or suggested by Garnett. For example, claim 9 recites a "microcontroller in the integrated circuit for receiving an encrypted bitstream" and "a configuration data register in the integrated circuit, wherein the configuration data register cannot be read by the microcontroller after the decryption program is used." Claim 12 recites "receiving an encrypted bitstream at a microcontroller within the field programmable gate array" and "loading a

configuration data register with a decrypted bitstream from the decryptor, wherein the configuration data register cannot be read by the microcontroller after the decryptor is used."

Claim 4 recites that the "decryptor is a software decryptor stored in a memory that uses hardware to enable access to the key storage register based on a memory address." Garnett does not teach or suggest this feature. At column 4, lines 10-21, Garnett teaches that a designer can utilize a design tool provided by the FPGA manufacturer to encrypt the configuration data set. The paragraph notes that the design tool can implement the inverse of the decryption algorithm embedded in the FPGA. As such, the cited paragraph deals with encrypting the configuration data set, not decryption. The paragraph is silent as to the decryptor being a software decryptor that uses hardware to enable access to the key storage register. Moreover, the paragraph makes no mention of enabling access to the key storage register based upon a memory address.

Claims 6 and 11 recite that "the microcontroller further receives a configuration boot program along with the encrypted bitstream." Item 4 of FIG. 6, which has been cited for teaching this feature, is a configuration data memory that is located "off-chip." The configuration data memory stores encrypted configuration information. Garnett does not teach or suggest that the microcontroller receives a configuration boot program. As noted, Garnett does not teach a microcontroller and, as such, would presumably have no need for a boot program. In any case, configuration data for programming a PLD is not equivalent to a boot program that can be executed by a microcontroller.

Claim 14 has been amended to correct a typographical error, as will be appreciated by those skilled in the art. Claim 14 further elaborates on the feature in which the configuration data register cannot be read by the microcontroller while the decryptor is in use. As noted, Garnett does not teach or suggest such a feature.

Claim 20 recites "a configuration boot program portion of the bitstream that runs a microcontroller on the programmable logic device," and "an encrypted bitstream portion of the bitstream containing encrypted configuration data that when decrypted and loaded into a configuration data register on the programmable logic device

configures the programmable logic device." As noted, Garnett does not teach or suggest a configuration boot program that runs on a microcontroller.

Claim 20 further recites that "the configuration boot program further comprises instructions for a decryptor, wherein the configuration boot program stores the instructions for the decryptor." Garnett also does not disclose that the configuration boot program includes instructions for the decryptor.

Claim 22 recites that the configuration boot program comprises instructions for a decompressor. Garnett does not teach or suggest such a feature.

The remaining claims rejected under Garnett are believed to be allowable in view of their own merits and further by virtue of their dependence upon underlying base claim(s) discussed above. As Garnett does not teach or suggest each limitation recited in the Applicants' claims, withdrawal of the 35 U.S.C. § 102(b) rejection of claims 1, 4-12, 14, and 20-22 is respectfully requested.

Rejections Under 35 U.S.C. § 103(a)

Claims 2, 3, 13, and 15-18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Garnett in view of U.S. Patent No. 6,366,117 to Pang et al. (Pang).

With respect to claim 2, the Office Action concedes that Garnett "does not disclose [that] the microcontroller stores key data in the key storage register, but the microcontroller cannot read from the key storage register." It is asserted, however, that Pang discloses this feature at items 26 and 29 of FIG. 3.

Pang does not disclose this limitation. First, it appears that the Office Action equates the configuration logic with the microcontroller. Applicants disagree and note that Pang does not explicitly teach a microcontroller as recited in Applicants' claims. Assuming arguendo that the configuration logic does include a microcontroller, Pang teaches only that one or more busses can be removed between the configuration logic and the key memory. Removal of bus 26, as taught by Pang, would prevent both storing and reading of the key memory by the configuration logic. Claim 2 recites that the microcontroller can store key data in the key storage register, but that the microcontroller cannot read from the key storage register. Modifying Garnett with the

teachings of Pang does not teach or suggest the embodiment recited in claim 2. In short, the microcontroller would not be able to read or write to the key storage register.

Claim 13 recites a similar feature in that claim 12 recites "wherein the configuration data register cannot be read by the microcontroller after the decryptor is used" and claim 13, which depends upon claim 12, recites that the method further comprises "loading the key register with key data from the microcontroller." Claim 13 is not taught or suggested by the combination of Garnett and Pang for the reasons noted above.

Claim 17 recites that "loading the decryptor with data from the key register and loading the decryptor with data from the microcontroller comprises using a predetermined instruction enabling access to the key storage register based on a known address of a memory storing a decryption engine forming the decryptor." The Office Action contends that this feature is taught by Garnett at column 4, lines 10-21 in reference to FIG. 4. As noted, Garnett does not teach or suggest that access to the key storage register can be enabled according to a known address of a memory that stores a decryption engine. The cited paragraph is silent as to this feature and makes no mention of an "address" or any dependency upon an address.

Claim 18 recites, in part, "logic circuitry limiting access to the key register from the microcontroller data bus using specified addresses of the non-volatile memory." The Office Action concedes that Garnett does not teach such a feature, but contends that Pang does at item 28 of FIG. 3. Item 28 is a bus linking the decryptor to the key memory. While Pang discloses a bus, Pang does not teach or suggest that access through the bus is limited or that the access via the bus is regulated using "specified addresses of the non-volatile memory." The Applicants request that a specific cite within Pang be provided as our review of the text accompanying FIG. 3 does not reveal such a feature.

The remaining claims rejected under the combination of Garnett and Pang are believed to be allowable in view of their dependency upon underlying base claim(s) and due to their own merits. In view of the foregoing, withdrawal of the 35 U.S.C. § 103(a) rejection of claims 2, 3, 13, and 15-18 is respectfully requested.

Claim 19 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Garnett and Pang in view of U.S. Patent No. 5,408,661 to Kuranaga (Kuranaga). The Office Action concedes that the combination of Garnett and Pang does not disclose that "the logic circuitry uses specified addresses of the non-volatile memory by limiting access to minimum and maximum ROM memory addresses using a microcontroller program counter." It is asserted, however, that Kuranaga does at column 6, lines 56-67.

As noted, Pang does not teach or suggest that access to the key register from the microcontroller is limited using specified addresses of the non-volatile memory. Kuranaga fails to cure this deficiency. At column 6, lines 56-67, Kuranaga discloses only that minimum and maximum virtual addresses of an instruction set can be stored in registers. Kuranaga, however, does not teach or suggest that a range of addresses for a microcontroller program counter can be used to limit access to the key register from the microcontroller. The cited passage of Kuranaga does not discuss limiting access to a key register or decryption.

As such, one attempting to solve the problems addressed by the embodiments of the Applicants' invention would not turn to Kuranaga for a solution, particularly in light of the deficiencies of both Garnett and Pang. Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection of claim 19 is respectfully requested.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on June 14, 2007.

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